REMARKS

Claims 1-115 are pending. In this Response, claims 101-115 have been added.

I. RESTRICTION REQUIREMENT

A Petition for Withdrawal of Restriction Requirement is filed herewith.

The Examiner asserts that "A complete response to the final rejection must include cancellation of non-elected claims or other appropriate action (see 37 CFR § 1.144 & MPEP § 821.01)." This is clearly erroneous. The outstanding Office Action is not final. Furthermore, the Petition for Withdrawal of Restriction Requirement is pending. Therefore, Applicant requests that the requirement for "cancellation of non-elected claims or other appropriate action" be withdrawn.

II. TITLE OBJECTION

The Examiner asserts that "The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed." This is clearly erroneous.

The Title is "Three-Dimensional Stacked Semiconductor Package Device with Bent and Flat Leads."

Claims 1-100 are directed to a three-dimensional stacked semiconductor package device that includes (1) a first semiconductor package device including (a) a first insulative housing, (b) a first semiconductor chip within the first insulative housing, and (c) a first lead that is bent downwardly outside the first insulative housing, (2) a second semiconductor package device that includes (a) a second insulative housing, (b) a second semiconductor chip within the second insulative housing, and (c) a second lead that is flat outside the second insulative housing, and (3) a conductive bond outside the insulative housings that contacts and electrically connects the leads.

Thus, the Title is clearly indicative of the invention to which the claims are directed.

Unfortunately, the Examiner has not provided any guidance as to how the Title is misdescriptive. Applicant suspects the Examiner insists that the Title account for method claims 91-100. In the interests of expediting the case, the Title has been amended in this manner. Therefore, Applicant requests that the Title objection be withdrawn.

III. SPECIFICATION CORRECTION

The Examiner requests Applicant's cooperation in correcting any errors of which Applicant may be aware in the Specification. Applicant is not aware of any errors in the Specification.

IV. SPECIFICATION OBJECTION

The Specification is objected to because Applicant's related applications information should be updated. The Specification has been amended in this manner. Therefore, Applicant requests that the Specification objection be withdrawn.

V. DRAWING OBJECTIONS – CLAIMS 1, 11, 21, 31, 41, 51, 61 AND 91

The drawings are objected to under 37 C.F.R. § 1.83(a) since the drawings must show every feature of the invention specified in the claims, and therefore various features must be shown or canceled from the claims.

The Examiner asserts that in claims 1, 11, 21, 31, 41, 51, 61 and 91, the limitations "the first semiconductor chip within the first insulative housing, wherein the first chip includes a first upper surface and a first lower surface, and the first upper surface includes a first conductive pad; and a first lead that protrudes laterally from and extends through the first peripheral side surface and is electrically connected to the first pad" and "a second semiconductor chip within the second insulative housing, wherein the second chip includes a second upper surface and a second lower surface, and the second upper surface includes a second conductive pad; and a second lead that protrudes laterally from and extends through the second peripheral side surface and is electrically connected to the second pad" are not shown in the drawings. This is clearly erroneous.

Semiconductor package device 186 is illustrated by its method of manufacture in Figs. 1A-18A and 1B-18B.

The method includes providing semiconductor chip 110 that includes upper surface 112 and lower surface 114, where upper surface 112 includes conductive pads 116 (Specification, page 12, lines 5-10 and Figs. 1A and 1B), providing metal base 120 that includes surfaces 122 and 124, central portion 126, slots 128, recessed portions 130, 132 and 134, non-recessed portions 136 and leads 138, where recessed portions 130 are formed in surface 122 and spaced from slots 128, recessed portions 132 are formed in surface 124 between slots 128, non-recessed portions 136 are formed between slots 128, and leads 138 include recessed portions 132 and non-recessed portions 136 (Specification, page 13, lines 1-11 and Figs. 2A and 2B), forming metal traces 144 on metal base 120, where metal traces 144 include terminals 146 in recessed portions 130 and routing lines 148 outside recessed portions 130 that extend to recessed portions 132, and conductive traces 150 include leads 138 and metal traces 144 (Specification, page 15, lines 5-18 and Figs. 3A and 3B), forming adhesive 154 on metal base 120 and metal traces 144 (Specification, page 17, lines 3-4 and Figs. 4A and 4B), mechanically attaching chip 110 to metal base 120 using adhesive 154 (Specification, page 17, lines 19-20 and Figs. 5A and 5B), forming encapsulant 156 on chip 110 and metal base 120, where encapsulant 156 includes top surface 160, peripheral side surfaces 162, bottom surface 164 and peripheral portion 166 (Specification, page 18, lines 15-16 and page 19, lines 11-13 and Figs. 6A and 6B), removing encapsulant 156 from laterally extending portions of slots 128 (Specification, page 29, lines 5-6 and Figs. 7A and 7B), forming protective coating 170 on metal base 120 outside encapsulant 156 (Specification, page 20, lines 21-22 and Figs. 8A and 8B), removing central portion 126 of metal base 120, thereby exposing terminals 146, routing lines 148 and adhesive 154 (Specification, page 21, lines 19-20 and 24 and Figs. 9A and 9B), forming openings 176 in adhesive 154 that expose pads 116 (Specification, page 22, lines 23-25 and Figs. 10A and 10B), forming connection joints 180 in openings 176 that contact and electrically connect pads 116 and routing lines 148 (Specification, page 23, lines 12-13 and Figs. 11A and 11B), forming insulative base 182 on the structure, where terminals 146 are exposed, and encapsulant 156 and insulative base 182 in combination form insulative housing 184 that surrounds and encapsulates chip 110 (Specification, page 24, lines

17-18 and 28-29 and page 25, lines 5-7 and Figs. 12A and 12B), singulating semiconductor package device 186 from the lead frame (Specification, page 25, line 26 to page 26, line 2 and Figs. 13A and 13B), bending leads 138 (Specification, page 26, lines 17-18 and Figs. 14A and 14B), and trimming semiconductor package device 186 (Specification, page 29, lines 3-4 and Figs. 15A and 15B).

Device 186 as shown in Figs. 13A and 13B includes chip 110, conductive traces 150, adhesive 154, connection joints 180 and insulative housing 184. Conductive traces 150 each include a lead 138 that protrudes laterally from and extends through a peripheral side surface 162 of insulative housing 184, a terminal 146 that protrudes downwardly from and extends through bottom surface 164 of insulative housing 184, and a routing line 148 within insulative housing 184 that is integral with an associated terminal 146 and contacts an associated lead 138 and connection joint 180. Conductive traces 150 are electrically connected to pads 116 by connection joints 180 in one-to-one relation, and are electrically isolated from one another. Leads 138 are arranged in opposing rows that protrude laterally from and extend through opposing peripheral side surfaces 162 and are disposed between top surface 160 and bottom surface 164. Terminals 146 are arranged as an array that protrudes downwardly from and extends through bottom surface 164 and is disposed inside inner side surfaces 174. Furthermore, leads 138 and terminals 146 are spaced and separated from one another outside insulative housing 184, and leads 138 and terminals 146 are electrically connected to one another and to pads 116 inside insulative housing 184 and outside chip 110. (Specification, page 26, lines 3-16.)

Thus, device 186 includes chip 110, conductive traces 150, connection joints 180 and insulative housing 184. Chip 110 is within insulative housing 184. Chip 110 includes upper surface 112 and lower surface 114, and upper surface 112 includes conductive pads 116. Conductive traces 150 each include a lead 138 that protrudes laterally from and extends through a peripheral side surface 162 of insulative housing 184. Conductive traces 150 are electrically connected to pads 116 by connection joints 180.

Three-dimensional stacked semiconductor package device 204 is shown in Fig. 19. Stacked device 204 includes device 186-3, device 186-4 and conductive bonds 202 (Specification, page 34, lines 22-23).

Device 186-3 is an untrimmed device 186 with bent leads composed of copper and no terminals, and device 186-4 is an untrimmed device 186 with flat leads composed of copper and shortened and no terminals. That is, device 186-3 is manufactured in accordance with Figs. 1-14 (without terminals 146, without protective coating 170 remaining on leads 138 and without the trimming operation in FIG. 15), and device 186-4 is manufactured in accordance with Figs. 1-13 (with shortened leads 138, without terminals 146, without protective coating 170 remaining on leads 138, without the lead bending operation in Fig. 14, and without the trimming operation in Fig. 15). As a result, device 186-3 is identical to device 186 in Figs. 14A and 14B except that the leads are copper and terminals 146 are omitted, and device 186-4 is identical to device 186 in Figs. 13A and 13B except that the leads are copper, the leads are shortened and terminals 146 are omitted. For convenience of illustration, the features of device 186-3 similar to those in device 186 have corresponding reference numerals with the suffix -3, and the features of device 186-4 similar to those in device 186 have corresponding reference numerals with the suffix -4. (Specification, page 32, lines 15-27.)

Device 186-3 includes leads 138-3 and insulative housing 184-3 with top surface 160-3, peripheral side surfaces 162-3 and bottom surface 164-3, and device 186-4 includes leads 138-4 and insulative housing 184-4 with top surface 160-4, peripheral side surfaces 162-4 and bottom surface 164-4. Leads 138-3 protrude laterally from and extend through opposing peripheral side surfaces 162-3 and are bent downwardly and extend downwardly beyond bottom surface 164-3 outside insulative housing 184-3, and leads 138-4 protrude laterally from and extend through opposing peripheral side surfaces 162-4 and are flat and do not extend downwardly beyond bottom surface 164-4 outside insulative housing 184-4. (Specification, page 33, lines 19-26.)

Thus, stacked device 204 includes devices 186-3 and 186-4.

Device 186-3 includes chip 110, conductive traces 150, connection joints 180 and insulative housing 184-3. Chip 110 is within insulative housing 184-3. Chip 110 includes upper surface 112 and lower surface 114, and upper surface 112 includes conductive pads 116. Conductive traces 150 each include a lead 138-3 that protrudes laterally from and extends through a peripheral side surface 162-3 of insulative housing 184-3. Conductive traces 150 are electrically connected to pads 116 by connection joints 180.

Device 186-4 includes chip 110, conductive traces 150, connection joints 180 and insulative housing 184-4. Chip 110 is within insulative housing 184-4. Chip 110 includes upper surface 112 and lower surface 114, and upper surface 112 includes conductive pads 116. Conductive traces 150 each include a lead 138-4 that protrudes laterally from and extends through a peripheral side surface 162-4 of insulative housing 184-4. Conductive traces 150 are electrically connected to pads 116 by connection joints 180.

In claims 1, 11, 21, 31, 41, 51, 61 and 91, the limitations are illustrated as follows: "the first semiconductor chip (110) within the first insulative housing (184-3), wherein the first chip (110) includes a first upper surface (112) and a first lower surface (114), and the first upper surface (112) includes a first conductive pad (116); and a first lead (138-3) that protrudes laterally from and extends through the first peripheral side surface (162-3) and is electrically connected to the first pad (116)" and "a second semiconductor chip (110) within the second insulative housing (184-4), wherein the second chip (110) includes a second upper surface (112) and a second lower surface (114), and the second upper surface (112) includes a second conductive pad (116); and a second lead (138-4) that protrudes laterally from and extends through the second peripheral side surface (162-4) and is electrically connected to the second pad (116)."

Semiconductor chip 110 with upper surface 112, lower surface 114 and conductive pad 116 within insulative housing 184 fully and clearly illustrates the first and second semiconductor chips within the first and second insulative housings, respectively. The Specification makes clear that devices 186-3 and 186-4 are identical to device 186 in this regard.

As a result, separate drawings for a first semiconductor chip (110-3) with a first upper surface (112-3), a first lower surface (114-3) and a first conductive pad (116-3) within the first insulative housing 184-3, as well as a second semiconductor chip (110-4) with a second upper surface (112-4), a second lower surface (114-4) and a second conductive pad (116-4) within the second insulative housing (184-4) are not only completely unnecessary, but also redundant and unenlightening and would needlessly clutter the captioned-application.

Furthermore, U.S. patents directed to three-dimensional stacked package devices often illustrate the internal structure of a single semiconductor package device as representative of other devices in the stack, rather than repeating the same illustration over-and-over for each device in the stack. See, for instance, *Choi* and *Kang* cited by the Examiner in the art rejections below.

Therefore, Applicant requests that this Drawing objection be withdrawn.

VI. DRAWING OBJECTIONS – CLAIMS 10, 20, 40, 50, 60 AND 100

The drawings are objected to under 37 C.F.R. § 1.83(a) since the drawings must show every feature of the invention specified in the claims, and therefore various features must be shown or canceled from the claims.

The Examiner asserts that in claims 10, 20, 40, 50, 60 and 100, the limitation "the stacked device is devoid of wire bonds and TAB leads" must be shown in the drawings. This is clearly erroneous.

These claims recite a negative limitation. Namely, the stacked device has no wire bonds and has no TAB leads. The M.P.E.P. sanctions negative limitations as follows:

> The current view of the courts is that there is nothing inherently ambiguous or uncertain about a negative limitation. So long as the boundaries of the patent protection sought are set forth definitely, albeit negatively, the claim complies with the requirements of 35 U.S.C. 112, second paragraph. (M.P.E.P. § 2173.05(i), Rev. 2, May 2004, page 2100-214.)

The Examiner's attempt to preclude Applicant from pursuing negative limitations under the guise that the negative limitations are not shown in the drawings is illogical and improper. This approach would abolish negative limitation practice.

Furthermore, the Specification Amendments list numerous U.S. patents that include this negative limitation in the claims without illustrating this negative limitation in the drawings. See, for instance, U.S. Patent Nos. 6,544,813; 6,548,393; 6,562,709; 6,576,539; 6,653,217; 6,660,626; 6,667,229; 6,673,710; 6,716,670 and 6,744,126. Examiners Berry, Clark, Dang, Lebentritt, Picardat, Richards and Rocchegiani had no problem allowing this negative limitation in these patents without illustrating this negative limitation in the drawings.

If the Examiner persists in this objection, perhaps the Examiner can enlighten Applicant as to how the drawings can illustrate the absence of wire bonds and TAB leads.

Therefore, Applicant requests that this Drawing objection be withdrawn.

VII. SECOND 112, SECOND PARAGRAPH REJECTIONS – CLAIMS 1, 11, 21, 31, 41, 51, 61 AND 91

Claims 1, 11, 21, 31, 41, 51, 61 and 91 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

The Examiner asserts that in claims 1, 11, 21, 31, 41, 51, 61 and 91, the limitations "the first semiconductor chip within the first insulative housing, wherein the first chip includes a first upper surface and a first lower surface, and the first upper surface includes a first conductive pad; and a first lead that protrudes laterally from and extends through the first peripheral side surface and is electrically connected to the first pad" and "a second semiconductor chip within the second insulative housing, wherein the second chip includes a second upper surface and a second lower surface, and the second upper surface includes a second conductive pad; and a second lead that protrudes laterally from and extends through the second peripheral side surface and is electrically connected to the second pad" are unclear and confusing to what is meant and where they are shown. This is clearly erroneous.

The limitations are clear and straightforward. Furthermore, the limitations are illustrated in the Drawings as discussed above.

Unfortunately, the Examiner has not provided any guidance as to what is unclear or confusing about these limitations.

Therefore, Applicant requests these rejections be withdrawn.

VIII. SECOND 112, SECOND PARAGRAPH REJECTIONS – CLAIMS 10, 20, 40, 50, 60 AND 100

Claims 10, 20, 40, 50, 60 and 100 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

The Examiner asserts that in claims 10, 20, 40, 50, 60 and 100, the limitation "the stacked device is devoid of wire bonds and TAB leads" is unclear and confusing to what is meant and where it is shown. This is clearly erroneous.

The limitation is clear and straightforward. Furthermore, the limitation is not and need not be illustrated in the Drawings as discussed above.

Unfortunately, the Examiner has not provided any guidance as to what is unclear or confusing about this limitation.

Furthermore, the Specification Amendments list numerous U.S. patents that include this negative limitation in the claims. See, for instance, U.S. Patent Nos. 6,544,813; 6,548,393; 6,562,709; 6,576,539; 6,653,217; 6,660,626; 6,667,229; 6,673,710; 6,716,670 and 6,744,126. Examiners Berry, Clark, Dang, Lebentritt, Picardat, Richards and Rocchegiani had no problem understanding this negative limitation in these patents.

Therefore, Applicant requests these rejections be withdrawn.

IX. SECTION 102 REJECTIONS – OHUCHI

Claims 1-7, 9-16 and 18-20 are rejected under 35 U.S.C. § 102(b) as being anticipated by *Ohuchi* (U.S. Patent No. 6,084,293).

Ohuchi discloses a stack type semiconductor device that includes semiconductor devices 3 and 40 and solder ball 42. Semiconductor device 3 includes lead 41. Semiconductor device 40 includes lead 21. Semiconductor device 40 is stacked on semiconductor device 3.

Semiconductor device 20 includes lead 21, solder ball 22, semiconductor element (chip) 23, resin (insulative housing) 24, insulating tape 25, conductor wire 27 and source line 28. Semiconductor element 23 includes terminal (pad) 26.

Semiconductor devices 3 and 40 are identical to semiconductor device 20, except that semiconductor device 3 is provided with lead 41 that lies astride the front and rear surfaces, and semiconductor device 40 is provided without solder ball 22. Thus, semiconductor device 3 includes semiconductor element 23, resin 24, insulating tape 25, conductor wire 27, source line 28 and lead 41, and semiconductor device 40 includes lead 21, semiconductor element 23, resin 24, insulating tape 25, conductor wire 27 and source line 28.

Claims 1 and 11 recite "a conductive bond . . . that extends laterally beyond any insulative material of the stacked device."

Ohuchi fails to teach or suggest this approach. Solder ball 42 does not extend laterally beyond resin 24 of semiconductor devices 3 and 40. Instead, resin 24 of semiconductor devices 3 and 40 extends laterally beyond solder ball 42.

The Examiner asserts that "Ohuchi . . . specifically figure 9 show . . . a first semiconductor package device 3 . . . a second semiconductor package device 40 . . . and a conductive bond 42 . . . that extends laterally beyond any insulative material of the stacked device." This is clearly erroneous. Solder ball 42 does not extend laterally beyond the insulative housings (resin 24) of semiconductor devices 3 and 40, as is apparent from Figs. 9 and 10.

Claims 1 and 11 also recite "a conductive bond . . . that . . . extends downwardly beyond a surface of the first chip."

Ohuchi fails to teach or suggest this approach. Solder ball 42 does not extend downwardly beyond a surface of semiconductor element 23 within semiconductor device 3. Instead, solder ball 42 is disposed above semiconductor element 23 within semiconductor device 3.

The Examiner asserts that "Ohuchi . . . specifically figure 9 show . . . a first semiconductor package device 3 . . . a second semiconductor package device 40 . . . and a conductive bond 42 . . . that . . . extends downwardly beyond a surface of the first chip." This is clearly erroneous. Solder ball 42 does not extend downwardly beyond a surface of semiconductor element 23 within semiconductor device 3, as is apparent from Figs. 4 and 9.

Accordingly, claims 1 and 11 distinguish over *Ohuchi.*

The dependent claims recite additional distinctions over *Ohuchi.*

Claims 2 and 12 recite "the first upper surface [of the first chip] [that includes the first conductive pad] faces towards the first bottom surface [of the first insulative housing]." *Ohuchi* fails to teach or suggest this approach. The upper surface of semiconductor element 23 within semiconductor device 3 does not face towards the bottom surface of resin 24 of semiconductor device 3. Instead, the upper surface of semiconductor element 23 within semiconductor device 3 faces towards the top surface of resin 24 of semiconductor device 3, as is apparent from Figs. 4 and 9. The Examiner asserts that "Ohuchi show wherein the first upper surface faces towards the first bottom surface." This is clearly erroneous.

Claim 5 recites "the first lead outside the first insulative housing includes inner and outer corners that are bent, an inner lateral portion that extends laterally between the first peripheral side surface and the inner corner, a sloped portion that extends laterally and downwardly between the inner and outer corners, and an outer lateral portion that extends laterally between the outer corner and a distal end." *Ohuchi* fails to teach or suggest this approach. Lead 41 outside resin 24 does not include a sloped portion that extends laterally and downwardly between inner and outer corners. Instead, lead 41 outside resin 24 includes a vertical portion that extends

downwardly (but not laterally) between the corners, as is apparent from Figs. 9 and 10. The Examiner asserts that "Ohuchi show wherein the first lead outside the first insulative housing includes inner and outer corners that are bent . . . [and] a sloped portion that extends laterally and downwardly between the inner and outer corners." This is clearly erroneous.

Claims 9 and 19 recite "the conductive bond has a substantially spherical shape." *Ohuchi* fails to teach or suggest this approach. Solder ball 42 does not have a substantially spherical shape after it is melted. Instead, solder ball 42 has a substantially hourglass shape after it is melted, as is apparent from Figs. 9 and 10. The Examiner asserts that "Ohuchi show wherein the conductive bond has a substantially spherical shape." This is clearly erroneous.

Claims 10 and 20 recite "the stacked device is devoid of wire bonds and TAB leads." *Ohuchi* fails to teach or suggest this approach. Semiconductor devices 3 and 40 are not devoid of wire bonds. Instead, semiconductor devices 3 and 40 include conductor wire (wire bond) 27. The Examiner asserts that "Ohuchi show wherein the stacked device is devoid of wire bonds and TAB leads as much as Applicant does." (Emphasis added.) This is clearly erroneous.

Under 35 U.S.C. § 102, anticipation requires that each and every element of the claimed invention be disclosed in the prior art. *Akzo N.V. v. United States International Trade Commission*, 1 USPQ 2d 1241, 1245 (Fed. Cir. 1986), *cert. denied*, 482 U.S. 909 (1987). That is, the reference must teach every aspect of the claimed invention. See M.P.E.P. § 706.02.

Ohuchi fails to teach or suggest limitations of independent claims 1 and 11 as well as various rejected dependent claims. Therefore, Applicant requests that these rejections be withdrawn.

X. SECTION 102 REJECTIONS – CHOI

Claims 1-6, 8, 11, 12, 14-18, 91-96 and 98 are rejected under 35 U.S.C. § 102(b) as being anticipated by *Choi* (U.S. Patent No. 6,190,944).

Choi discloses a stacked semiconductor package that includes first-type package P1, second-type package P2 and solder 30. Package P1 includes chip 31, lead 33, wire 34 and

molding portion 36. Chip 31 includes pad 32, and lead 33 includes outer lead 33b with uppermost surface 33c. Package P2 includes chip 131, lead 133, wire 134 and molding portion 136. Chip 131 includes pad 132, lead 133 includes chip-attached portion 133a, substrate-attached portion 133b and connecting portion 133c, and substrate-attached portion 133b includes bottom surface 133d.

Package P2 is stacked on package P1. Leads 33 and 133 are "welded" by solder 30. Further, molding portions 36 and 136 are adhered by an adhesive (not shown) therebetween.

Claims 1, 11 and 91 recite "a conductive bond . . . that . . . extends downwardly beyond a surface of the first chip."

Choi fails to teach or suggest this approach. Solder 30 does not extend downwardly beyond a surface of chip 31. Instead, solder 30 is disposed above chip 31.

The Examiner asserts that "Choi . . . specifically figure 3A show . . . a first semiconductor chip (31 within P1) . . . and a conductive bond 30 . . . that . . . extends downwardly beyond a surface of the first chip." This is clearly erroneous. Solder 30 does not extend downwardly beyond a surface of chip 31, as is apparent from Fig. 3A.

Accordingly, claims 1, 11 and 91 distinguish over *Choi.*

The dependent claims recite additional distinctions over *Choi.*

Claims 2, 12 and 92 recite "the first upper surface [of the first chip] [that includes the first conductive pad] faces towards the first bottom surface [of the first insulative housing]." *Choi* fails to teach or suggest this approach. The upper surface of chip 31 does not face towards the bottom surface of molding portion 36. Instead, the upper surface of chip 31 faces towards the top surface of molding portion 36, as is apparent from Fig. 3A. The Examiner asserts that "Choi show wherein the first upper surface faces towards the first bottom surface." This is clearly erroneous.

Claims 5 and 95 recite "the first lead outside the first insulative housing includes inner and outer corners that are bent, an inner lateral portion that extends laterally between the first peripheral side surface and the inner corner, a sloped portion that extends laterally and downwardly between the inner and outer corners, and an outer lateral portion that extends laterally between the outer corner and a distal end." *Choi* fails to teach or suggest this approach. Lead 33 outside molding portion 36 does not include a sloped portion that extends laterally and downwardly between inner and outer corners. Instead, lead 33 outside molding portion 36 is shaped in the 'J' type, as is apparent from Fig. 3A. The Examiner asserts that "Choi show wherein the first lead outside the first insulative housing includes inner and outer corners that are bent . . . [and] a sloped portion that extends laterally and downwardly between the inner and outer corners." This is clearly erroneous.

Claims 8, 17 and 98 recite "the conductive bond is outside the peripheries of the insulative housings." *Choi* fails to teach or suggest this approach. Solder 30 is not outside the peripheries of molding portions 36 and 136. Instead, solder 30 extends within the peripheries of molding portions 36 and 136, as is apparent from Fig. 3A. The Examiner asserts that "Choi show wherein the conductive bond is outside the peripheries of the insulative housings." This is clearly erroneous.

Claim 17 also recites "the conductive bond is spaced from the insulative housings." *Choi* fails to teach or suggest this approach. Solder 30 is not spaced from molding portion 36. Instead, solder 30 contacts molding portion 36, as is apparent from Fig. 3A. The Examiner asserts that "Choi show wherein the conductive bond is spaced from the insulative housings." This is clearly erroneous. Furthermore, claims 7 and 97 recite this limitation but are not rejected over *Choi*.

Claim 18 recites "the conductive bond contacts only the leads." *Choi* fails to teach or suggest this approach. Solder 30 does not contact only leads 33 and 133. Instead, solder 30 also contacts molding portion 36, as is apparent from Fig. 3A. The Examiner asserts that "Choi show wherein the conductive bond contacts only the leads." This is clearly erroneous.

Under 35 U.S.C. § 102, anticipation requires that each and every element of the claimed invention be disclosed in the prior art. *Akzo N.V. v. United States International Trade Commission*, 1 USPQ 2d 1241, 1245 (Fed. Cir. 1986), *cert. denied*, 482 U.S. 909 (1987). That is, the reference must teach every aspect of the claimed invention. See M.P.E.P. § 706.02.

Choi fails to teach or suggest limitations of independent claims 1, 11 and 91 as well as various rejected dependent claims. Therefore, Applicant requests that these rejections be withdrawn.

XI. SECTION 103 REJECTIONS – KANG

Claims 1-8, 11-18, 31-39, 41-48, 51-58 and 91-98 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Kang* (U.S. Patent No. 6,242,285).

Kang discloses a stacked package that includes lower semiconductor package IC_A, upper semiconductor package IC_B and solder 70. Lower semiconductor package IC_A includes leads $P15_A$ and $P19_A$, and upper semiconductor package IC_B includes leads $P15_B$ and $P19_B$. Upper semiconductor package IC_B is stacked on lower semiconductor package IC_A. Furthermore, upper semiconductor package IC_B has its leads deformed in the shape of an approximately conventional dual inline package (DIP) so that stacking can be achieved.

Upper semiconductor package IC_B includes inner die (chip) 100_B, bonding wire 319_B, leads 415_B and 419_B (similar to leads $P15_B$ and $P19_B$, respectively) and molding compound 500_B. Inner die 100_B includes chip selection (CS) pad 219_B. Lead $P15_B$ is a no connection (NC) lead, that is, lead $P15_B$ is not wire bonded to any pad on the inner die. Lead $P19_B$ is a chip selection (CS) lead, that is, lead $P19_B$ is wire bonded to CS pad 219_B.

Lower semiconductor package IC_A is identical to upper semiconductor package IC_B.

In the stacked package, upper semiconductor package IC_B is modified so that (1) leads $P15_B$ and $P19_B$ are electrically connected together, and (2) lead $P19_B$ is vertically shortened. As a result, lower semiconductor package IC_A has lead $P19_A$ connected to the CS pad of its inner die and lead $P15_A$ is disconnected from its inner die, and upper semiconductor package IC_B has leads

$P15_B$ and $P19_B$ connected to the CS pad of its inner die. Furthermore, leads $P15_A$ and $P15_B$ are soldered together, but leads $P19_A$ and $P19_B$ are not soldered together.

During operation, if the CS signal is applied to lead $P19_A$ then lower semiconductor package IC_A is activated but upper semiconductor package IC_B is deactivated since leads $P19_A$ and $P19_B$ are disconnected. Likewise, if the CS signal is applied to leads $P15_A$ and $P15_B$ then upper semiconductor package IC_B is activated since leads $P15_B$ and $P19_B$ are connected together but lower semiconductor package IC_A is deactivated since lead $P15_A$ is a NC lead.

Kang emphasizes the importance of bending lead $P15_B$ to provide the stacked package:

> However, to form a stacked package, the leads $P1_B$ through $P27_B$ of the upper semiconductor device IC_B are deformed in the shape of an approximately conventional DIP (Dual Inline Package) lead. (Column, 4, lines 39-43.)

Kang also emphasizes the importance of keeping lead $P19_B$ short so that leads $P19_A$ and $P19_B$ are disconnected:

> Referring to FIG. 4A, the length of the outer connection portion of the 419_B lead is shortened and intentionally disconnected from the CS lead 419_A of the lower semiconductor package IC_A. (Column, 7, lines 19-22.)

Kang also emphasizes the importance of keeping leads $P15_A$ and $P15_B$ close together so that solder 70 is small and forms a good connection:

> As depicted, the leads $P27_A$ and $P27_B$ of the upper and lower semiconductor packages IC_B and IC_A are connected by a soldering in which a conductive material having a good conductivity is used as a soldering material. When soldering, when a spacing between the two leads $P27_A$ and $P27_B$ is a minimum distance, e.g. about 0.3 mm or less, the soldered material under the influence of a surface tension force and so forth forms a connection ball naturally. The connection ball produced at the natural state is good in its connection state and has a good conductivity. (Column, 6, lines 11-20.)

Claims 1, 11, 31, 41 and 51 recite "the second lead outside the second insulative housing is flat." Likewise, claim 91 recites "the second lead remains flat outside the insulative housings."

Kang fails to teach or suggest this approach. Lead $P15_B$ outside molding compound 500_B is not flat. Instead, lead $P15_B$ outside molding compound 500_B is bent. Furthermore, there is no teaching, suggestion or motivation to flatten lead $P15_B$ outside molding compound 500_B, particularly since *Kang* teaches away from this.

The Examiner asserts that "Kang . . . specifically figures 4A and 4B show . . . a second lead {upper flat portion (P1(subB)-P18(subB)) and (P19(sub B)-P27(subB))} that . . . outside the second insulative housing is flat; and a conductive bond{side flat portion (P1(subB)-P18(subB)) and (P19(sub B)-P27(subB)) and 70}." This is clearly erroneous. Lead $P15_B$ includes the upper flat portion and the side flat portion, as is apparent from Figs. 4A and 4B.

The Examiner also asserts that "the 35 U.S.C. § 103 rejection based on a second lead and a conductive bond deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts." (Emphasis in original.)

The Examiner's position is vague and confusing.

The Examiner's remarks about *Kang* characterize the upper flat portion of lead $P15_B$ as the "the second lead outside the second insulative housing" and the side flat portion of lead $P15_B$ and solder 70 as the "conductive bond . . . [that] contacts and electrically connects the leads." However, the Examiner fails to propose any modification to *Kang*. As best Applicant can tell, the Examiner asserts that the claims read on *Kang* without modifying *Kang*, but this doesn't make sense under a Section 103 rejection.

The Examiner's remarks about the case law mention the second lead, the conductive bond and "the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece." However, the Examiner fails to propose any modification to *Kang*. As best Applicant can tell, the Examiner proposes modifying *Kang* by eliminating the side flat portion of lead $P15_B$ and having solder 70 contact and electrically connect lead $P15_A$ and the

upper flat portion of lead $P15_B$. But this doesn't make sense since *Kang* teaches that lead $P15_B$ must be bent for stacking, and leads $P15_A$ and $P15_B$ must be spaced by minimum distance so that solder 70 provides a good connection. This also doesn't make sense since *Kang* teaches that lead $P19_B$ is shortened at its side flat portion so that it is "intentionally disconnected" from lead $P19_A$. Thus, *Kang* teaches away from the proposed modification.

Applicant should be given a reasonable explanation of what the proposed modification is rather than be forced to second-guess what it is. For this reason alone, the rejection is improper and should be overturned.

Moreover, the proposed modification, insofar as it can be understood, has no motivation, is not taught or suggested by *Kang*, is taught away from by *Kang* and would render *Kang* unsatisfactory for its intended purpose.

Accordingly, claims 1, 11, 31, 41, 51 and 91 distinguish over *Kang*.

The claims recite additional distinctions over *Kang*.

Claims 2, 12, 32, 42, 52 and 92 recite "the first upper surface [of the first chip] [that includes the first conductive pad] faces towards the first bottom surface [of the first insulative housing]." *Kang* fails to teach or suggest this approach. The upper surface of the inner die of lower semiconductor package IC_A does not face towards the bottom surface of the molding compound of lower semiconductor package IC_A. Instead, the upper surface of the inner die of lower semiconductor package IC_A faces towards the top surface of the molding compound of lower semiconductor package IC_A, as is apparent from Figs. 2E and 4A. The Examiner asserts that "Kang show wherein the first upper surface faces towards the first bottom surface." This is clearly erroneous.

Claims 3 and 93 recite "the second lead does not extend downwardly beyond the second bottom surface outside the second insulative housing." Likewise, claims 11 and 51 recite "the second lead outside the second insulative housing . . . does not extend downwardly beyond the second bottom surface." *Kang* fails to teach or suggest this approach. Lead $P15_B$ extends downwardly beyond the bottom surface of molding compound 500_B outside molding compound

500_B, as is apparent from Figs. 4A and 4B. The Examiner asserts that "Kang show wherein . . . the second lead does not extend downwardly beyond the second bottom surface outside the second insulative housing." This is clearly erroneous.

Claims 6, 16, 45, 55 and 96 recite "the second lead outside the second insulative housing is essentially identical to the inner lateral portion of the first lead." *Kang* fails to teach or suggest this approach. Lead $P15_B$ outside molding compound 500_B is not essentially identical to the inner lateral portion of lead $P15_A$ [that extends laterally outside the molding compound of lower semiconductor package IC_A between the peripheral side surface of the molding compound of lower semiconductor package IC_A and an inner corner of lead $P15_A$ outside the molding compound of lower semiconductor package IC_A]. Instead, lead $P15_B$ outside molding compound 500_B is markedly different than the inner lateral portion of lead $P15_A$, as is apparent from Figs. 4A and 4B. The Examiner asserts that "Kang show wherein the second lead outside the second insulative housing is essentially identical to the inner lateral portion of the first lead." This is clearly erroneous.

Claims 14, 33, 43 and 53 recite "the first lead is adjacent to the first bottom surface, and the second lead is adjacent to the second bottom surface." *Kang* fails to teach or suggest this approach. Lead $P15_A$ is not adjacent to the bottom surface of the molding compound of lower semiconductor package IC_A, and lead $P15_B$ is not adjacent to the bottom surface of the molding compound (500_B) of upper semiconductor package IC_B, as is apparent from Figs. 2E, 4A and 4B. The Examiner asserts that "Kang show wherein the first lead is adjacent to the first bottom surface, and the second lead is adjacent to the second bottom surface." This is clearly erroneous.

Claims 36, 46 and 56 recite "the conductive bond is laterally aligned with the second bottom surface." *Kang* fails to teach or suggest this approach. Solder 70 is not laterally aligned with the bottom surface of molding compound 500_B, as is apparent from Figs. 4A and 4B. The Examiner asserts that "Kang show wherein the conductive bond is laterally aligned with the second bottom surface." This is clearly erroneous.

Claim 38 recites "the conductive bond contacts only the inner lateral portion and the second lead." *Kang* fails to teach or suggest this approach. Solder 70 does not contact only the

inner lateral portion of lead $P15_A$. Instead, solder 70 also contacts additional portions of lead $P15_A$, as is apparent from Fig. 3. The Examiner asserts that "Kang show wherein the conductive bond contacts only the inner lateral portion and the second lead." This is clearly erroneous.

To establish prima facie obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. See M.P.E.P. § 2142.

It is insufficient that the prior art shows similar components unless it also contains some teaching, suggestion or incentive for arriving at the claimed structure. See *Northern Telecom, Inc. v. Datapoint Corp.*, 908 F.2d 931, 934 (Fed. Cir. 1990).

Moreover, if the proposed modification would render the prior art unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. See M.P.E.P. § 2143.01.

Kang fails to teach or suggest limitations of independent claims 1, 11, 31, 41, 51 and 91 as well as various rejected dependent claims, and the proposed modification fails to cure this deficiency. Therefore, Applicant requests that these rejections be withdrawn.

XII. SECTION 103 REJECTIONS – KANG AND YAMAZAKI ET AL.

Claims 9, 19, 39, 49, 59 and 99 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Kang* in view of *Yamazaki et al.* (U.S. Patent Application Publication No. 2001/0054762).

Applicant submits these rejections are moot for the reasons set forth above.

XIII. SECTION 103 REJECTIONS – CHOI AND YAMAZAKI ET AL.

Claims 9, 19, 39, 49, 59 and 99 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Choi* in view of *Yamazaki et al.*

Applicant submits these rejections are moot for the reasons set forth above.

XIV. SECTION 103 REJECTIONS – OHUCHI AND OSAWA

Claims 10, 20, 40, 50, 60 and 100 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ohuchi* in view of *Osawa* (Japanese Patent Publication No. 06-097352).

Applicant submits these rejections are moot for the reasons set forth above.

XV. SECTION 103 REJECTIONS – KANG AND OSAWA

Claims 10, 20, 40, 50, 60 and 100 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Kang* in view of *Osawa*.

Applicant submits these rejections are moot for the reasons set forth above.

XVI. SECTION 103 REJECTIONS – CHOI AND OSAWA

Claims 10, 20, 40, 50, 60 and 100 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Choi* in view of *Osawa*.

Applicant submits these rejections are moot for the reasons set forth above.

XVII. NEW CLAIMS

Claims 101-115 have been added to further explicate various features of the invention. No new matter has been added.

Claim 101 recites "the conductive bond is solder." The Specification provides support at page 43, lines 20-29.

Claim 102 recites "the conductive bond is a solder ball ." The Specification provides support at page 44, lines 15-23.

Claim 103 recites "the conductive bond is conductive adhesive." The Specification provides support at page 44, lines 1-10. *Ohuchi*, *Choi* and *Kang* fail to teach or suggest this approach, and *Yamazaki et al.* and *Osawa* fail to cure this deficiency.

Claim 104 recites "conductive adhesive that includes an epoxy binder and silver flakes." The Specification provides support at page 44, lines 1-10. *Ohuchi*, *Choi* and *Kang* fail to teach or suggest this approach, and *Yamazaki et al.* and *Osawa* fail to cure this deficiency.

Claim 105 recites "the conductive bond is a solder-coated copper ball." The Specification provides support at page 44, lines 24-30. *Ohuchi*, *Choi* and *Kang* fail to teach or suggest this approach, and *Yamazaki et al.* and *Osawa* fail to cure this deficiency.

Claim 106 recites "the conductive bond includes solder that contacts the leads and a copper ball that is coated by the solder." The Specification provides support at page 44, lines 24-30. *Ohuchi*, *Choi* and *Kang* fail to teach or suggest this approach, and *Yamazaki et al.* and *Osawa* fail to cure this deficiency.

Claim 107 recites "the conductive bond extends downwardly beyond the first chip." The Specification provides support at Figs. 7D and 19. *Ohuchi*, *Choi* and *Kang* fail to teach or suggest this approach, and *Yamazaki et al.* and *Osawa* fail to cure this deficiency.

Claim 108 recites "the conductive bond does not extend upwardly beyond any surface of the second chip." The Specification provides support at Figs. 7D and 19. *Kang* (with the Examiner's improper characterization of the conductive bond) fails to teach or suggest this approach, and *Yamazaki et al.* and *Osawa* fail to cure this deficiency.

Claim 109 recites "the conductive bond extends downwardly beyond the first chip and does not extend upwardly beyond any surface of the second chip." The Specification provides support at Figs. 7D and 19. *Ohuchi*, *Choi* and *Kang* fail to teach or suggest this approach, and *Yamazaki et al.* and *Osawa* fail to cure this deficiency.

Claim 110 recites "the conductive bond does not extend upwardly beyond the second lead." The Specification provides support at Fig. 19. *Kang* fails to teach or suggest this approach, and *Yamazaki et al.* and *Osawa* fail to cure this deficiency.

Claim 111 recites "the conductive bond does not extend upwardly beyond the second bottom surface." The Specification provides support at Fig. 19. *Kang* (with the Examiner's improper characterization of the conductive bond) fails to teach or suggest this approach, and *Yamazaki et al.* and *Osawa* fail to cure this deficiency.

Claim 112 recites "the conductive bond does not extend upwardly beyond any surface of the second device." The Specification provides support at Fig. 19. *Ohuchi* and *Kang* fail to teach or suggest this approach, and *Yamazaki et al.* and *Osawa* fail to cure this deficiency.

Claim 113 recites "the conductive bond extends vertically across essentially all of the first device and extends vertically across essentially none of the second device." The Specification provides support at Fig. 19. *Ohuchi*, *Choi* and *Kang* fail to teach or suggest this approach, and *Yamazaki et al.* and *Osawa* fail to cure this deficiency.

Claim 114 recites "the first device is a single-chip package, the second device is a single-chip package, and the conductive bond includes solder or conductive adhesive and extends downwardly beyond the first chip and does not extend upwardly beyond any surface of the second chip." The Specification provides support at page 32, lines 22-27, page 43, lines 20-29, page 44, lines 1-10, and Figs. 5A, 7D and 19. *Ohuchi*, *Choi* and *Kang* fail to teach or suggest this approach, and *Yamazaki et al.* and *Osawa* fail to cure this deficiency.

Claim 115 recites "the conductive bond includes solder or conductive adhesive and extends vertically across essentially all of the first device and extends vertically across essentially none of the second device." The Specification provides support at page 43, lines 20-29, page 44, lines 1-10, and Fig. 19. *Ohuchi*, *Choi* and *Kang* fail to teach or suggest this approach, and *Yamazaki et al.* and *Osawa* fail to cure this deficiency.

XVIII. FEES

The fee for this Response is calculated below:

For	Claims Remaining After Amendment	Highest Number Previously Paid For		Extra Claims	Rate		Additional Fee
Total Claims	205	- 100	=	105	x $9	=	$945
Independent Claims	10	- 10	=	0	x $43	=	$0
Multiple Dep. Claim	1	0			x$145	=	$145
Total Fee						=	$1090

Please charge the $1090 fee to Deposit Account No. 502178/BDG005-6 and charge any underpayment or credit any overpayment to this Account.

XIX. CONCLUSION

In view of the remarks set forth herein, the application is believed to be in condition for allowance. Should any issues remain, the Examiner is encouraged to telephone the undersigned attorney.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on September 13, 2004

D Sigmond

David M. Sigmond
Attorney for Applicant

9/13/04
Date of Signature

Respectfully submitted,

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TITLE AMENDMENTS

Replace the Title with the following Title:

THREE-DIMENSIONAL STACKED SEMICONDUCTOR PACKAGE DEVICE WITH BENT AND FLAT LEADS AND METHOD OF MAKING SAME